STATUS OF THE CLAIMS

Claims 1-11 were originally filed in this patent application. In response to the Examiner's rejections, claims 1, 4, and 7 were amended in an amendment dated 09/15/05. Further, claims 12-14 were added in the same amendment. In the previous office action, claims 1-14 were rejected under 35 U.S.C. §112, first and second paragraphs, and claims 1-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,050,070 to Chastain *et al.* (hereinafter "Chastain") in view of Brenner *et al.* (hereinafter "Brenner"). No claim was allowed. In the most recent office action, claims 7-14 were rejected under 35 U.S.C. §101, and claims 1-14 were rejected under 35 U.S.C. §112, second paragraph, and claims 1-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,912,533 to Hornick in view of Barabash *et al.* (hereinafter "Barabash"). No claim was allowed. Claims 1-7 and 10-11 have been amended herein and claims 8 and 9 have been cancelled. Claims 1-7 and 10-14 are currently pending.

REMARKS

Rejection of claims 7-14 under 35 U.S.C. §101

The Examiner rejected claims 7-14 as being directed to non-statutory subject matter. Claim 7 has been amended and claims 8 and 9 were cancelled to overcome this rejection. Applicant respectfully requests the Examiner to reconsider the rejection under U.S.C. §101.

Rejection of claims 1-14 under 35 U.S.C. §112, second paragraph

The Examiner has rejected the claims as being indefinite. As to claims 1, 4 and 7, these claims have been amended to overcome this rejection by replacing references to an additional thread to the new thread. The amendments have also been reflected in the references to the claims in the discussion below. Applicant respectfully requests the Examiner to reconsider the rejection under U.S.C. §112 second paragraph.

As to claims 12-14, these claims have not been amended to overcome this rejection. The terms of first and second thread are different from the new thread. These terms are used to introduce additional limitations to the claims. These claims recite a first thread for each processor, and that all processors are made busy with a first thread before dispatching a second thread to any processor. Claims 12-14 are not indefinite because the relationship between the two threads and the other claim language is clear. Applicant respectfully requests the Examiner to reconsider the rejection under U.S.C. §112 second paragraph.

Rejection of claims 1-14 under 35 U.S.C. §103(a)

The Examiner rejected claims 1-14 under 35 U.S.C. §103(a) as being unpatentable over the combination of Hornick and Barabash. Applicant traverses the Examiner's finding of obviousness and believes the cited art, singularly or in combination does not teach or suggest the invention in the pending claims.

Hornick teaches a system that allocates data mining processing tasks among multiple computer systems and/or among multiple processors. Barabash teaches a task dispatcher that dispatches tasks to processors that have a task identification queue. Neither Hornick or Barabash deal with hardware multithreading as claimed herein.

Claim 1

Claim 1 includes the limitation that the thread dispatch mechanism determines which of the processors is busy processing a thread but can accept a new thread. The combination of the cited art does not teach or suggest to distinguish between a processor that is busy and cannot accept a new thread and one that is busy but can accept a new thread. The cited art does not deal with a processor that has hardware multithreading as recited in the claims.

For the limitation of "determining which of the plurality of processors is busy processing a thread but can accept a new thread", the Examiner has cited Hornick col 12, lines 40-42. Applicant can find no such teaching in this portion of Hornick. The cited section teaches determining if a computer is relatively not busy compared to another computer system. This does not teach or suggest anything about hardware multithreading in a processor. A processor that is busy but can accept a new thread is a processor that has processing capability for multiple hardware threads. Hornick is not concerned with processors that have hardware multithreading. In Hornick the system determines the

relative busy status of the processor by looking at the processing load (col. 12, line 47). The processing load is not related to whether a processor is busy but can accept a new thread. The processing load in Hornick is related to the typical situation of software multitasking. This is evident in Hornick where all the references are to tasks and queues in memory and not threads and processor hardware.

The cited art does not teach or suggest to differentiate between a processor that is idle, one that is busy but can accept a new thread, and one that cannot accept a new thread. In the cited art, there is no hardware support for hardware multithreading, so there are only two states of a processor: idle, meaning the processor is doing nothing; or busy, meaning the processor cannot accept a new thread. In the claims, the dispatch mechanism determines if a processor is busy, whether it is busy but can accept a new thread, or whether it can't accept a new thread. The cited art does not teach or suggest to make this distinction over three possible states of the processor. Since Hornick and Barabash do not teach or suggest to determine whether a processor is busy but can accept a new thread, claim 1 is allowable over the combination of Hornick and Barabash. Applicant respectfully requests reconsideration of the rejection of claim 1 under 35 U.S.C. §103(a).

Further, claim 1 has the limitation of a processor "having hardware support for the capability of executing a plurality of threads". For this limitation, the Examiner has cited Hornick col 8, lines 33-36. The cited art does not teach or suggest that the processors have hardware support to execute a plurality of threads. The cited portion of Hornick deals with multiple processors, while claim 1 includes hardware support for multiple threads for a single processor. Hornick does not deal with multiple hardware threads at all. Executing multiple tasks from a queue is not the same as dispatching multiple threads to a multi-threaded processor (processor having hardware support for the capability of executing a plurality of threads). Those of ordinary skill in the art would not mix up or equate these terms in the context of the claim language. The cited art is simply not that relevant to hardware multithreading and describes something quite different than

the claimed invention. The Examiner's rejection relies on reading claim terms beyond their ordinary meaning as used in the art. The Examiner has failed to establish a prima facie case of obviousness under 35 U.S.C. §103(a). Reconsideration of the rejection is respectfully requested.

Claim 1 also has the limitation of a processor "cannot accept a new thread since it is working on a maximum number of threads the processor can execute". For this limitation, the Examiner has cited Hornick col 12, lines 44-45. This section of the Hornick deals with the relative busy condition of the computer system. The cited section does not teach or suggest anything about a maximum number of threads the processor can execute. The Examiner's logic makes a huge leap that is without support in the cited art. The Examiner or the cited art does not show any logical tie between relatively busy and the maximum number of threads the processor can execute. The logical tie between relative busy and maximum number of threads is lacking even if threads were the same as tasks as the Examiner apparently has assumed (wrongfully as discussed above). Relatively busy is related to how many tasks are in a queue, but that says nothing about a maximum number of threads (or even the number of tasks in the queue). Here again, the Examiner has failed to establish a prima facie case of obviousness under 35 U.S.C. §103(a). Reconsideration of the rejection is respectfully requested.

Claim 2

Claim 2 depends on claim 1, which is allowable for the reasons given above. As a result, claim 2 is allowable as depending on an allowable independent claim. Further, claim 2 contains an additional claim limitation that is not taught or suggested by the cited art. For claim 2 the Examiner cited Hornick, col. 11 lines 26-49. Applicant has not found anything in the cited section, or in Hornick in general to support the Examiner's rejection. The cited sections of Hornick do not teach or suggest "if none of the plurality of processors is idle and if at least one of the plurality of processors can accept a new thread,

the thread dispatch mechanism dispatches the new thread to one of the plurality of processors that can accept a new thread." As discussed above, Hornick does not address hardware threads at all. In Hornick, the tasks are stored in queues. Applicant respectfully requests the Examiner to reconsider the rejection of claim 2 under 35 U.S.C. §103(a).

Claim 3

Claim 3 depends on claim 1, which is allowable for the reasons given above. As a result, claim 3 is allowable as depending on an allowable independent claim. Further, with regards to the rejection of claim 3, the Examiner states that Hornick discloses the limitation of "the thread dispatch mechanism waits for one of the plurality of processors to complete processing" recited in claim 3, citing Hornick's Figure 8. Applicant has not found this teaching in Figure 8, or any other portion of Hornick. In Figure 8, if an agent is busy then the process finds the first available agent to process the mining task. There is no discussion in Hornick concerning waiting for a processor to become a processor that can accept a thread. Hornick deals with queues of software tasks. Since Hornick and Barabash do not teach or suggest to wait until a processor can accept a new thread, Applicant respectfully requests reconsideration of the rejection of claim 3 under 35 U.S.C. §103(a).

Claims 4-11

Claim 4 and 7 contain similar limitations to those described above with reference to claim 1. Therefore claims 4 and 7 are also allowable over the cited art. Further, claims 5-6 and 8-11 depend on claims 4 and 7 respectively, which are allowable for the reasons given above. As a result, claims 5-6 and 8-11 are allowable as depending on allowable independent claims.

Claims 12-14

Claims 12-14 depend on claims 1, 4 and 7 respectively, which are allowable for the reasons given above. As a result, claims 12-14 are allowable as depending on allowable independent claims. Further, with regards to the rejection of claim 12, the Examiner states that Barabash discloses the limitation of "making all the processors busy with a first thread before dispatching an additional thread" recited in claim 3, citing Barabash col.6, line 40 - col. 7, line 14. There is no discussion in Barabash concerning a making all the processors busy with a first thread before dispatching an new thread to the processor. Barabash deals with queues of tasks and teaches making all processors busy with a first task and then sending additional tasks **to a queue**. Since Hornick and Barabash do not teach or suggest to make all the processors busy with a first thread before dispatching a new thread **to the processor**, Applicant respectfully requests reconsideration of the rejection of claims 12-14 under 35 U.S.C. §103(a).

Conclusion

In summary, none of the cited prior art, either alone or in combination, teach, support, or suggest the unique combination of features in applicant's claims presently on file. Therefore, applicant respectfully asserts that all of applicant's claims are allowable. Such allowance at an early date is respectfully requested. The Examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

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Respectfully submitted,

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